A
REAL TIME
INFRARED ARRAY IC

By

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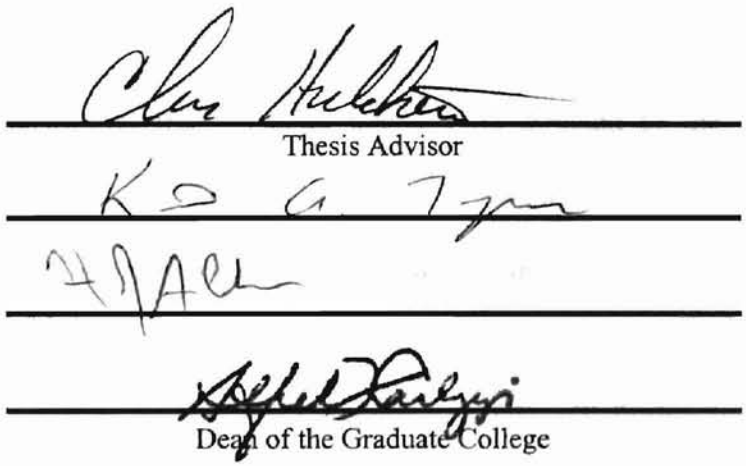

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PREFACE

The objective of the Real Time Infrared System Test Set (RTIR) project is to develop a cost effective, compact, portable, rugged, and reliable prototype for use of all levels of readiness testing. RTIR develops and employs a silicon-based micro-machined Complementary Metal Oxide Semiconductor (CMOS) electronic-driven array of IR heater elements. The Thermal Pixel Array (TPA) devices are designed to have response times suitable for real-time scene generation.

In the near future, RTIR application will be directed to the requirements to support Navy missile simulation systems and for incorporation into existing rate tables for missile flight testing. The RTIR capability will reduce the number of test systems in the maintenance chain for IR sensors, thus lowering the overall system cost of operation. The potential of RTIR as built-in-test-equipment (BITE) will further improve readiness testing by providing an on-board method of end-to-end system test for expensive sensors and weapon systems.

The 128 by 128 RTIR array is design to operate at up to 100Hz, and at temperatures up to 700Kelvin. The major advancement of RTIR project includes industrial fabrication (mass produce) of arrays with small enough dimensions to accommodate the large number of pixels, and the use of high resistance polysilicon material for heater element, the temperature range is maximized and the current requirement is minimized.

ACKNOWLEDGMENTS

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NOMENCLATURE

ΔI_D	change in DC diode current
τ	time constant of switch
ε	full settling error
ΔI_{room}	change in temperature between room and operational temperature
C_{store}	storage capacitor in the pixel cell
$D_0 \ldots D_{15}$	16 bits digital address
DAC	Digital-to-analog converter
I_ε	error current
I_D	DC current flow through diode
I_{Dleak}	leakage current of the pixel diode
I_{pix}	current supply to the pixel element
I_S	diode saturation current
I_{source}	current source
I_{swleak}	leakage current of the switch
I_o	output current
M1	pixel drive transistor
M_{Diode}	diode connected MOS
R_{pix}	pixel element
R_{sw}	on resistance of the switch
T_e	emitter temperature
V_{bias}	bias voltage of cascoded transistor
V_{Brk}	transistor breakdown voltage
V_D	diode voltage

V_{Dbias}	diode bias voltage
V_{dd_d}	digital power suppl
V_{DDPIX}	analog power supply
V_{Diode}	diode connected MOS voltage
V_{Droop}	droop voltage
V_{DS}	drain to source voltage
V_{GS1}	gate to source voltage of drive transistor
VINB	input voltage of the test setup
V_o	pixel output voltage
V_{peak}	peak voltage
V_{ss_d}	digital ground
V_{sspix}	analog ground
V_{store}	voltage stored on to the pixel capacitor
V_T	diode thermal equivalent voltage
W_E	write enable signal

CHAPTER 1

INTRODUCTION

The objective of the 10-bit grayscale Real Time Infrared Array (RTIR) project is to develop a reliable prototype infrared (IR) test set for the use in calibration and testing of IR imaging systems, including built in test to ensure the real-time reliability of IR sensing systems. The IC resulting from the RTIR project will support offensive and defensive weapons testing, surveillance, and guidance applications throughout the Navy, such as Navy missile simulation systems and IR seekers. The potential of the RTIR as built-in-test-equipment (BITE) is in its potential to reduce the number of test systems in the maintenance chain for IR sensor and guidance systems, thus lowering the overall system cost of operation.

An IR scene IC has been constructed that can accurately reproduce real-time, static or dynamic infrared images, which utilizes standard silicon-based micromachining techniques. The RTIR IC along with a compact electronics subsystem based on a standard desktop PC greatly reduce the complexity of the required external support electronics resulting in a smaller, inexpensive, easily used, and maintained, real-time

scene generator system. The IC consists of a data input block, address write control, pixel-specific electronics including a micro-heater suspend over a micromachined silicon substrate cavity. Current is passed through the polysilicon emitter resistors that heat up to generating the thermal images. The display IC consists of an array of 128 x 128 resistive emitters arranged as a 16 element analog write by 1024. The pixel cell power dynamic range is maximized at 1mA of input current, and it is designed to achieve 9 bits of write accuracy. The Thermal Pixel Array (TPA) elements have response times less than a millisecond making them suitable for real-time scene simulation. The design specification of the RTIR array is shown in table I.

Emitter array resolution	128 x 128 pixels
Pixel Pitch	88.6 micron
Heater element size	40 microns square
Operation temperature range	300K~800K (Heater)
Response Time constant (rise)	2.0ms (air)
Response Time constant (fall)	0.7ms (air)
Maximum refresh rate	100 Hz (10mSec Hold)
Max Pixel Current	500uA
Input Data	10 Bits analog current
TPA Digital Power	5 VDC
TPA Pixel Power	5 - 8 VDC

Table I. Thermal Pixel Array (TPA) Design Specification

An IR scene generator is not unique [1, 2, 3, 4, 5, 6], however, its fabrication on monolithic silicon substrate utilizing a standard commercial IC process is a first which over time and volume yields lower costs of production. Other researchers have produced other integrated solutions, but their success has depended on specialized processing techniques, which adds significantly to the cost of production. For example, Honeywell's Infrared (IR) night-vision imaging systems are at present too costly to allow widespread commercial applications. Its chip requires cryogenic coolers and/or specialized IR sensor materials and customized process. Honeywell uses the monolithic silicon fabrication of the Two-level Microbolometer (stack die/Multi Chip Module) Pixel and the chip operates at a slower refresh rate (compare to the RTIR IC designed here) at about 30Hz [7].

For a cost-effective approach, IR scene generator arrays must be small and mass-produceable. A combination of Commercial CMOS process and MEMS technology have being chosen as a cost effective technique to thermally isolated the infrared emitter microstructure from substrate electronics. Fabrication of a RTIR IC using commercial CMOS technology consists of two parts: (1) a implementation layout design is prepared using a CAD tool and submitted to the IC foundry for fabrication; (2) after receiving the wafers from the IC foundry, an anisotropic etching is performed at SPAWAR's Integrated Circuit Research and Fabrication Branch to create the free standing microstructures, suitable for infrared scene generation. The 1.2 micron Supertex (formerly Orbit Semiconductor) CMOS BULK process was selected to fabricate the 128 by 128 array of electronically addressable 40 x 40 microns emitter elements (Fig. 1). The availability of a high value poly resistor provides lower pixel current operation while preserving the pixel dynamic range.

1.1 Post-Processing

In order to create the thermal isolation for the pixels, a post-fabrication anisotropic etching is performed on the wafer. The anisotropic etchant removes the substrate through the opening created by the special layout design (Fig. 1) [8, 9]. The thermal pixel consists of a polysilicon heater element, sandwiched between two silicon layers and is suspended by four diagonal supports over an anisotropically etched cavity. The micromachined cavity is constructed by using a silicon etchant that undercuts the desired pattern in the silicon substrate, while leaving it electrically connected to create a suspended structure/micro-heater (Fig. 2) [10] which provides the thermal isolation for the heater element by reducing the heat conducted to the substrate. This pattern is created by patterning and plasma etching silicon dioxide thereby exposing the substrate silicon of the CMOS chip. The exposed silicon is then exposed to a Tetra-methyl ammonium hydroxide (TMAH) solution, an anisotropic silicon etchant. Potassium Hydroxide (KOH) and EDP can also be used as crystallographic etchants of silicon but both are hazardous to work with, and KOH attacks metal, which would remove metal from the bonding pads on the CMOS chip. TMAH was chosen for the following reasons: (a) it is commonly used to etch silicon wafers, (b) it is less hazardous then other etchants, (c) literature suggests that a solution could be made with TMAH that did not attack metal [11], and (d) it is readily available. The TMAH etch can be achieve by a simple lab setup [8,9].

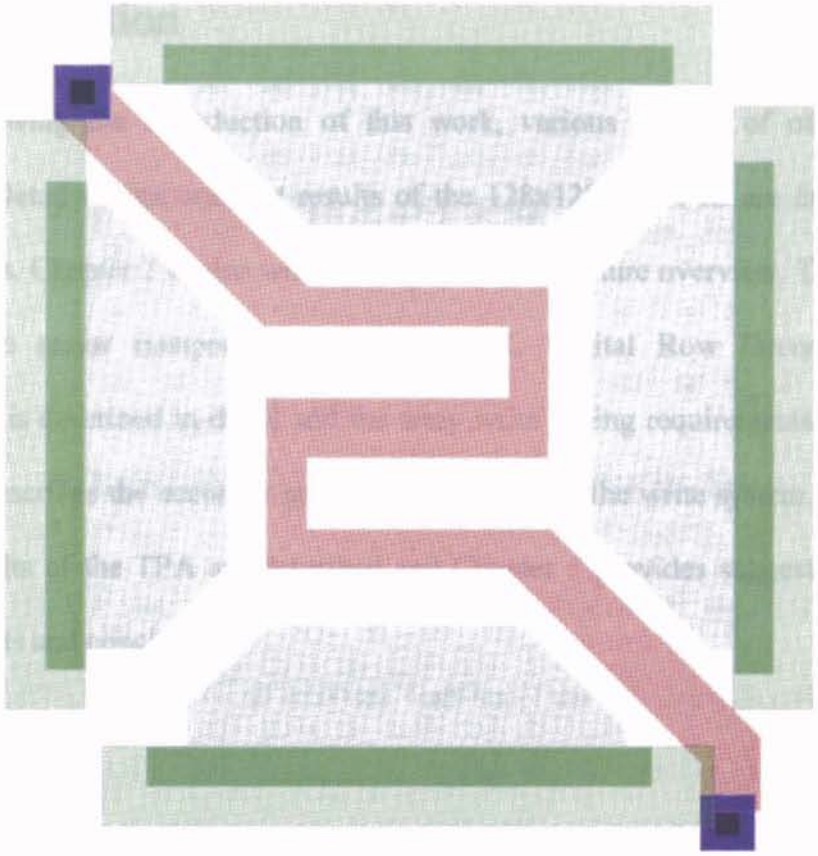

Fig. 1: The 40 x 40 microns heater element layout

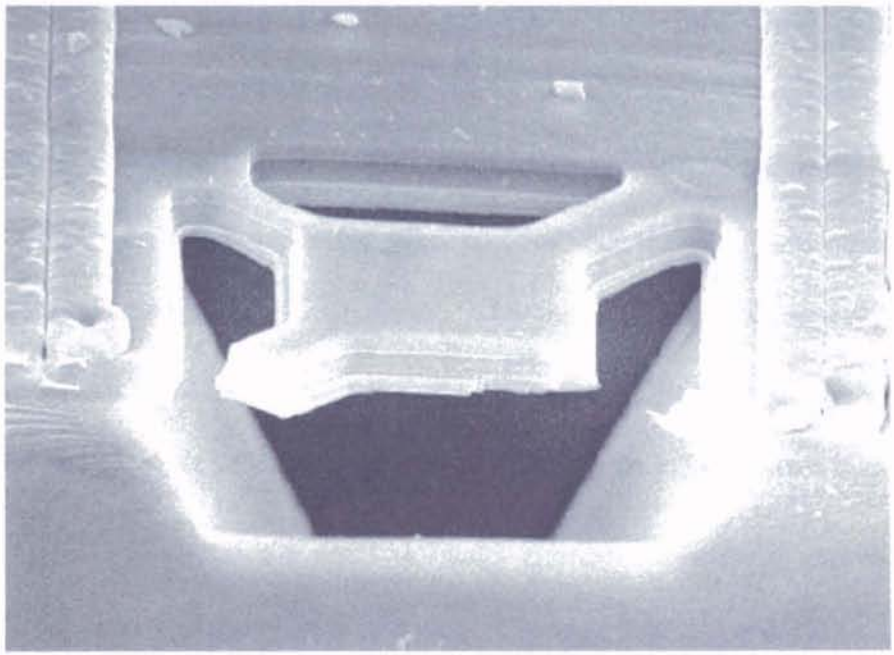

Fig. 2: SEM of a cross-sectioned sample of a suspended microheater. Isolation has been fully achieved and layered oxide structures are visible

1.2 Organization

Following the introduction of this work, various aspects of other works are reviewed. Detail design and test results of the 128x128 RTIR IC are described in the later chapters. Chapter 2 begins with the RTIR IC architecture overview. The architecture of the three major components (Analog MUX, Digital Row Decoder and Pixel Electronics) is described in detail and the array write timing requirements are discussed. Chapter 3 describes the accuracy performance factors of the write system. In Chapter 4, the test results of the TPA are described and Chapter 5 provides suggestions for future improvements and conclusion.

CHAPTER 2

SYSTEM ARCHITECTURE OVERVIEW

The 128x128 RTIR IC architecture consists of the following key blocks shown in Figure 3: analog column multiplexer (data inputs), digital row decoder, and an array of heater elements surrounded by the pixel-specific electronics that allow for rapid loading and retention of data. The pixel information is written using a 16-element word. Each of the 16 column banks consists of a 1:8 column decoder. A Single word write will send data to one of the 8 outputs of each of the 16 column decoders (banks). Input data ($D_0 \ldots D_{15}$) are a 0-1mA current. The pixel intensity is controlled by varying the magnitude of a current flowing in the pixel resistor and, thereby, varies the intensity of thermal energy radiated from each pixel. The input data are steered through a 1:8 transmission gate analog multiplexer to one of 8 outputs with three LSB address bits. A 1:128 digital row decoder provides selection with the seven MSB address bits.

The pixel cell contains a resistive heater element (or infrared emitter), a storage capacitor, pixel drive transistors and switches. The user digitally specifies a specific row and column and then writes a pixel current to the desired cell via the analog mux. The

infrared pixel array IC is designed for use in conjunction with a computer, or with a specific electronic controller, which is designed to service or update real-time images. The computer sends gray scale scene data to the pixel array in the form of currents, which the IR pixel array displays as a gray scale image. The computer controls digital row and column address lines as well as writes analog inputs via the DAC to the RTIR IC. The current magnitude reflects the desired IR intensity of the pixel element thereby achieving the gray scale levels. After writing to the pixel, the desired voltage is stored dynamically for greater than 10msec with less than 0.1% droop producing the desired IR pixel intensity while the remaining pixels are updated. The key blocks are custom designed to meet the specification in Table I from chapter 1.

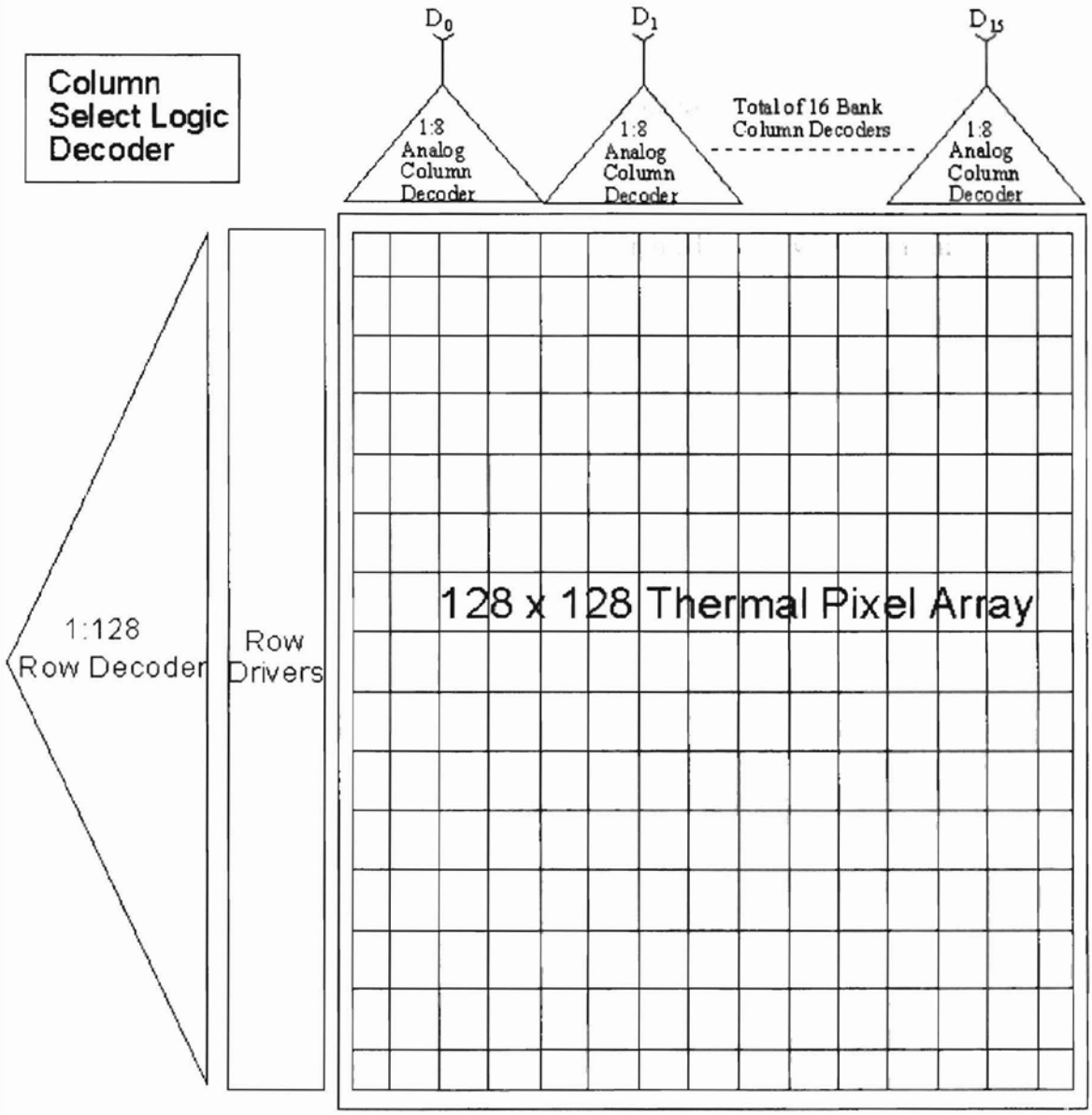

Fig. 3: Floorplan of the Real Time Infrared Array IC

2.1 COLUMN DECODER (ANALOG MUX)

The dual path analog mux is a pair of standard tree-decoders – with a dedicated current return path (i.e. dedicated input to output current path) that has one active output and input connection with all other pathways in the high impedance state (see pixel write mechanism in Fig. 8). To reduce write times, decoder area, and decoder routing complexity, the 128 actual pixel columns have been segmented into 16 'banks', each 8 pixels wide. The column decoder is a 1:8 decoder made of NMOS transmission gates (Fig 4.), which are suitable for passing current unidirectionally.

The analog decoder accepts an analog current input and delivers it to one of 8 output ports. The write circuitry consists of a dynamic current mirror with the input "MOS diode" present in each column and the mirror transistors present in each pixel. The input current for each of the 16 banks is then steered to a column current mirror diode, and the desired current is then mirrored into each pixel element. The dynamic mirror has the advantages of storing a voltage on the gate to source, which reflects both the write currents as well as the pixel currents [12]. In addition, the gate to source capacitance need not be linear or long term stable. All 128 columns of pixels are supported by each column write diode.

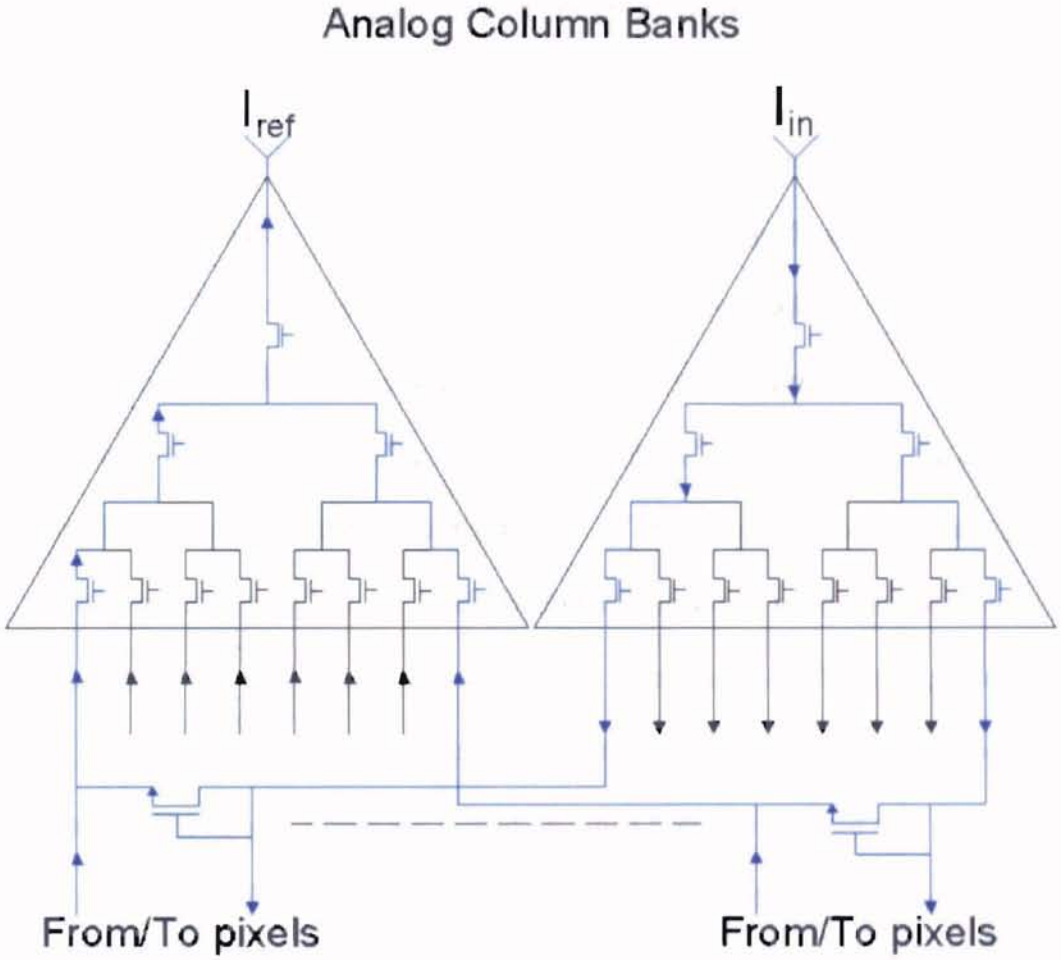

Fig. 4: One pair of the 1:8 analog mux. One bank provides the input path and the other provides the reference path. Duplicate multiplexers were included for signal balancing

2.2 ROW DECODER

The 1:128 digital transmission gate decoder provides random access row selection. Decoding is followed by a NAND gate and row driver. The NAND gate shown in Fig. 5 allows W_E to gate the row selection to control write timing. Two 1:64 decoders are combined with a 1:2 decoder to achieve the 1:128 decoder. Each 1:64 decoder utilizes two different versions of the 1:8 decoder, one being the logical complement of the other. The input of the 1:2 decoder (Fig. 5) is connected to ground and inverted to a "1" by inverters between the 1:8 decoders inside the 1:64 decoder block. Inverters were placed between stages of the decoders to optimize the decoding delay. One version of the 1:2 decoder (Fig. 6) is used for the 1^{st} to 4^{th} levels of the decoder with one of the inputs permanently connected to V_{dd_d}. The second version of the 1:2 decoder (Fig. 7) is used for the 5^{th} to 7^{th} levels of the 1:8 decoder, which connects one of the inputs to digital ground (V_{ss_d}) permanently. The purpose of having two different decoders is to allow for the existence of the optimizing delay inverters between the 4^{th} and 5^{th} layer. The row switches are turned on when both the W_E and row decoder output are true. A Super buffer is added at the output of each NAND gate to drive the 128 rows of pixels.

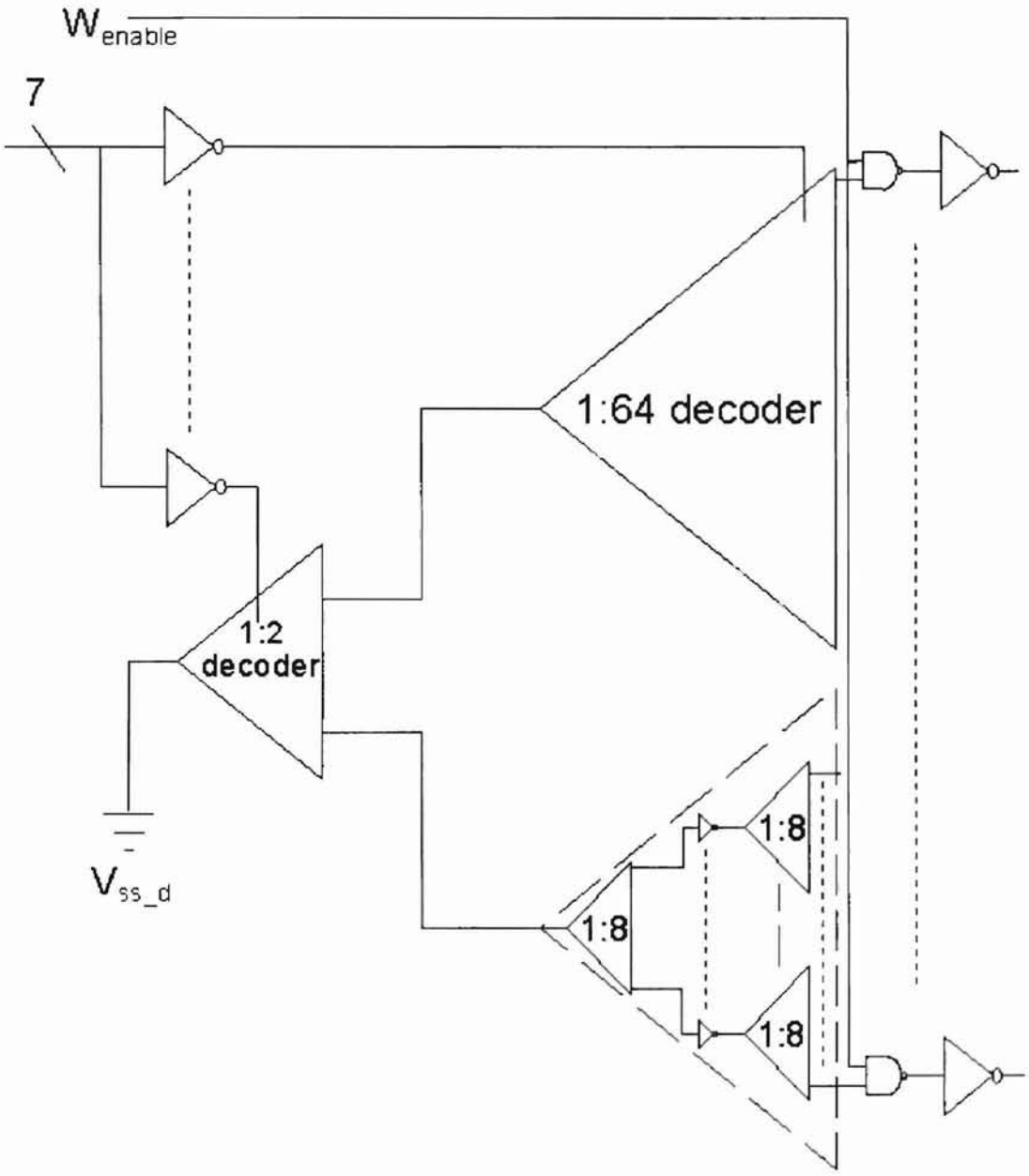

Fig. 5: Row decoder block diagram

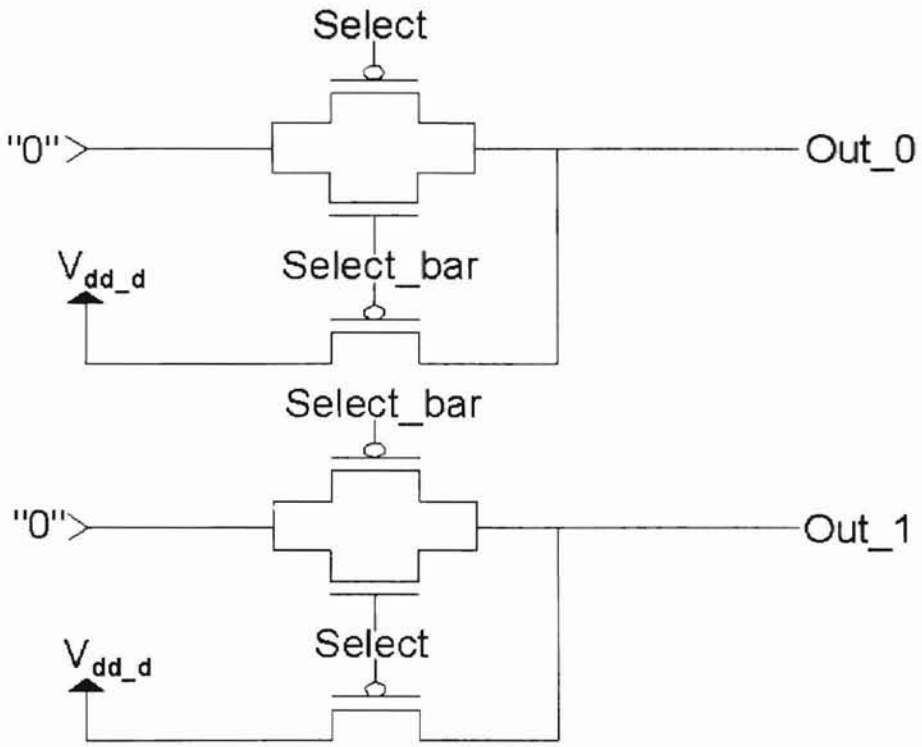

Fig. 6: The 1:2 decoder with input tie to V_{dd_d} and passing "0"

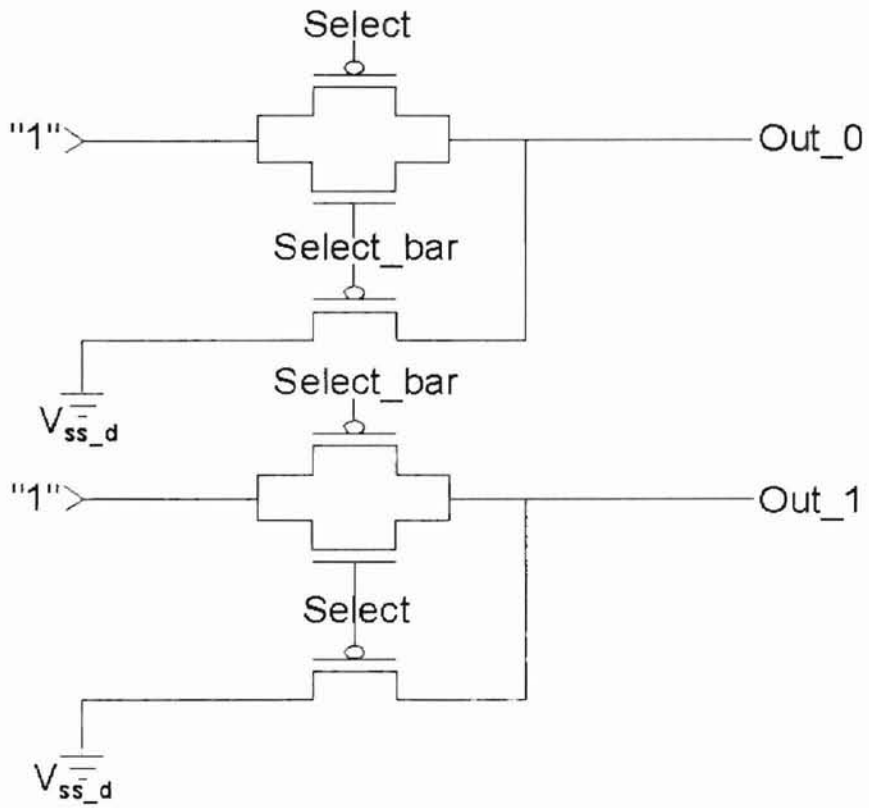

Fig. 7: The 1:2 decoder with input tie to V_{ss_d} and passing "1"

2.3 PIXEL ELECTRONICS

The pixel write system (Fig. 8) consists of an analog input current (0~1mA) which is scaled and mirrored to the pixel element's NMOS cascode transistors with a current range of 0~0.5mA (a mirrored current ratio of 2:1). The row and column select switches allow the gate voltage of the diode-connected transistor (M_{Diode}, resident at the top of each column) to be written into the selected pixel by storing the voltage on to the capacitor (C_{store}). The column "diode" (M_{Diode}), drive transistor (M1) and C_{store} comprise a dynamic current mirror. The voltage stored on the capacitor (V_{GS1}) maintains the pixel current through the pixel resistor after the write cycle. The gate voltage (V_{bias}) of M2 is held at a level to ensure proper cascoding of M1. Cascoding of the drive transistor (M1) ensures reduced fluctuations in the IR emission level but increasing the output impedance.

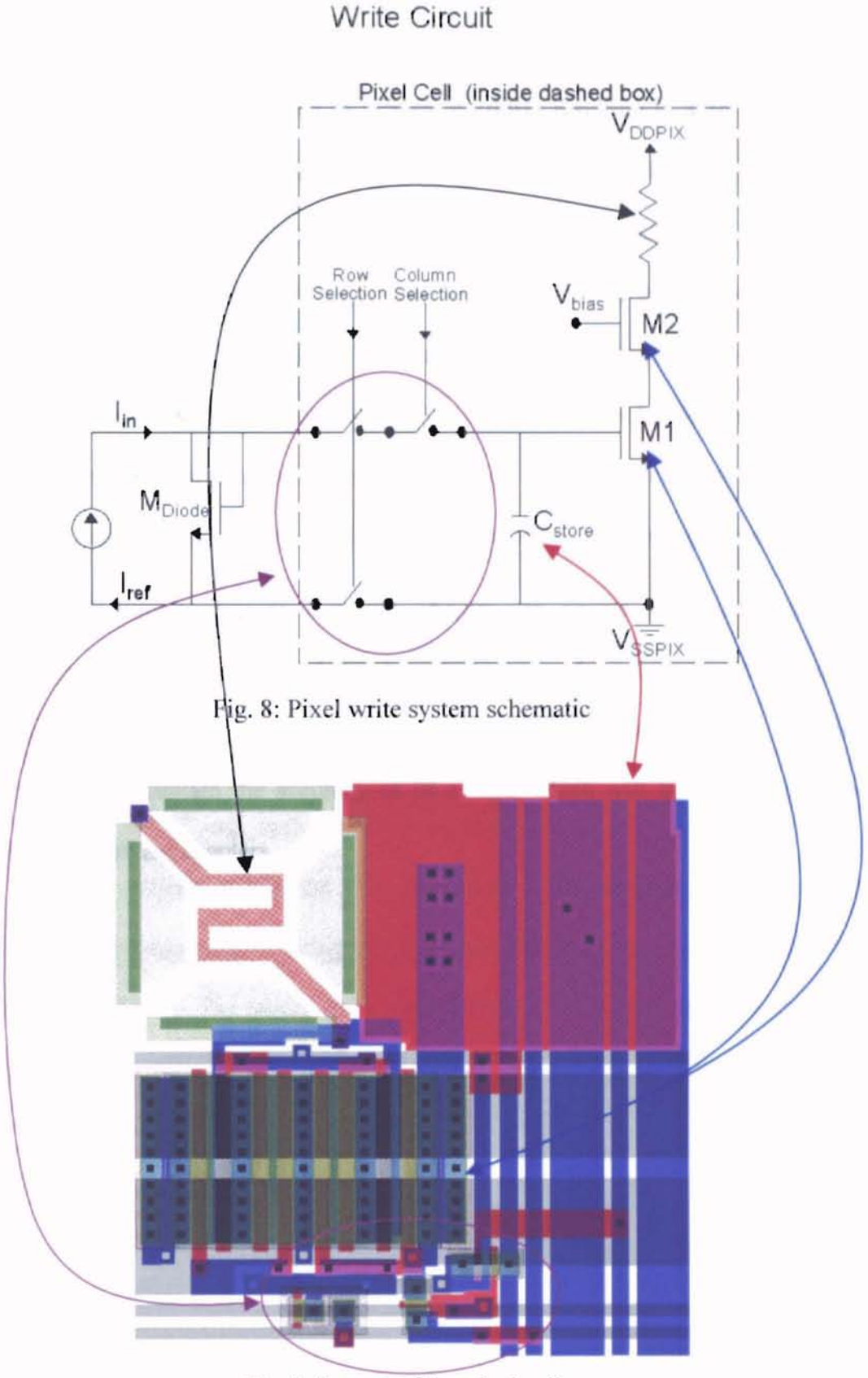

Fig. 8: Pixel write system schematic

Fig. 9: Layout of the pixel cell

2.4 WRITE TIMING

The entire array is designed to refresh at 100Hz resulting in a 16 element word with a write time of less than 2μsec. The write enable (W_E) must be valid for 1.8μsec to ensure accurate settling. The write enable is applied 100nsec after the application of Address and Data, and removed 100nsec prior to the removal of Address and Data. The Analog Data must be held valid while W_E is true and Data is assumed to be "latched" on the trailing edge of W_E. This write procedure ensures that only the desired cells are modified. The column selection is removed prior to row selection to avoid charge injection into the pixel capacitor as the column selection switch is being turned off.

The IC circuits presented in this chapter are simple standard circuits with customized geometry and optimized speed to meet or exceed the design specification. To make sure the information being written is maintained between each refresh, techniques were adopted to maintain the accuracy of IR image, which will be discussed in more detail in the following chapters.

CHAPTER 3

ACCURACY AND PERFORMANCE FACTORS

Several issues related to accuracy and performance of the RTIR chip, and techniques to solve or investigate these issues are discussed in this chapter. During the write cycle, the analog current is being written to the pixels. To ensure the information is written correctly, the following requirements must be considered: (a) the matching of the column "diode MOS" and each pixel's drive transistor in the column (mismatched mirror), (b) full settling, and (c) the IR voltage drop. Post write, the time between each refresh (the time information is being held), requires that the droop caused by the leakage current be minimized. The nonlinearity of the emitter (R_{pix}) associated with temperature is an un-modeled issue along with thermal cross talk that effects the IR image accuracy.

3.1 WRITE ISSUE

The distribution of the drive transistors across this large chip entails a number of important issues to be addressed including: (a) the matching between each column "diode MOS" and the drive transistors in a column; (b) full settling; and (c) the IR voltage drops along the write path, including the reference path and power buses. The mismatch between I_{source} and I_{pix}, as a result of the mismatch between the M_{Diode} and M1 which results in a variation between the stored pixel voltage (current) within the array and the desired voltage. For the large number of drive transistors connected to the same ground line, the systematic mismatch between the current sources and mirrored current may not be consistent throughout the chip which may resulted an unacceptable mismatch. As a result, these errors must be designed to calibrate by preprocessing or prewarping the scene image. To partially remedy these performance issues a local reference is employed in each pixel cell for a source current to return to the signal return path, I_{ref} in Fig. 10. The two row-write switches were included inside each pixel cell to provide the write through and the return path to eliminate the effects of power supply bow while providing local referencing of the stored analog information.

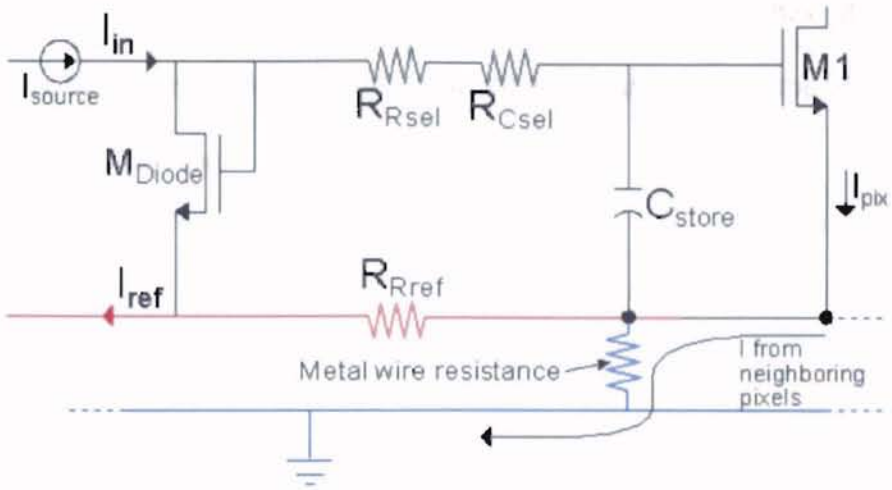

Fig. 10: The pixel write path

The present of the added I_{ref} return path eliminates the image dependent IR voltage fluctuation caused by the neighboring pixels. After write, the voltage of C_{store} (V_{store}) equals to the difference of V_{Diode} and $I(R_{Rref}+R_{Rsel}+R_{Csel})$ (when the switches are opened). As the capacitor reaches steady state and current flow approaches zero, V_{store} is approximately equal to the diode voltage (V_{Diode}) as t approaches infinity, thus minimizing the $3IR_{sw}$ voltage drop. As a result the only remaining uncontrolled error terms are due to mismatch of geometry, doping and temperature variation across the array.

Write accuracy is a function of the settling time. Since the RTIR chip operates at 100Hz, the time allowed for each pixel to write and hold must be less than 10 msec. Equation (1) shows the exponential increase in voltage (V_o) when writing to the pixel where τ is the time constant for the column and row select switches in the pixel cell which equals to $3R_{sw}C_{store}$. The difference between the fully charged voltage and the desired voltage level is the error term (ε) given in equation (2) where n is the number bits of accuracy. To find the settling time required, substitute (1) into (2) and solving for t

which results in (3). From (3), the geometry of the three switches, the size of the capacitor (set by the thermal noise floor and allowable droop) and the allowable droop determine the settling time.

$$V_o = V(1 - e^{-\frac{t}{\tau}}) \tag{1}$$

$$V_o - V \le \varepsilon = V/2^{n+1} \tag{2}$$

$$t = \tau \ln 2^{n+1} \tag{3}$$

To improve write accuracy, it is essential that the ground plane bow be minimized. In large ICs, the DC or transient voltage drop along the buses may be significant, affecting sensitive analog circuits supplied by the same power bus. Furthermore, eletromigration mandates a minimum line width to guarantee long-term reliability. The IR voltage drop in the ground plane is minimized by reducing I_{pix} which in turn requires R_{pix} to be increased. Equation (4) is the pixel power dissipation and in (5) V_{DDPIX}, the required power supply voltage, is equal to the high resistance poly heater element drop, $R_{pix}I_{pix}$, plus the $2\Delta V$ of the cascoded transistors. V_{DDPIX} must be less than transistor's breakdown voltage (V_{Brk}) to ensure proper operation.

$$P_{pixel} = I^2 R_{pix} \tag{4}$$

$$V_{DDPIX} = IR_{pix} + 2\Delta V < V_{Brk} \tag{5}$$

Using power equals to $\frac{V_{DDPIX}^{2}}{R_{pix}}$, replacing V_{DDPIX} by V_{Brk} and solving for I results in (6).

$$I < \frac{V_{Brk} - 2\Delta V}{R_{pix}} \tag{6}$$

or solving for R_{pix} in (7)

$$R_{pix} < \frac{V_{Brk} - 2\Delta V}{I} \tag{7}$$

The heater element resistance is set by a combination of the process breakdown, the trampoline area of the heater element, limits of poly doping, and IR emission requirement. Given a pixel resistor value (R_{pix}) of 15K ohms along with the 60dB of dynamic range objective demands pixel current sink output resistance in excess of 1Meg ohms. This in turn requires the cascoding of M1 in Fig. 12. While pixel cell storage capacitance must be greater than 240fFd for purpose of suppressing thermal noise, a poly1 to poly2 1100fFd hold capacitor was used to minimize droop. The pixel capacitor was designed as large as the available pixel wiring area after the power buses widths were determined. Fig. 8 shows the schematic of the pixel cell along with the layout shown in Fig. 9 from chapter 2.

3.2 DROOP ISSUE

The current must be held accurate to 1 part per 1000 for more than 10msec (during the post write or hold phase). To minimize droop over time, a diode is added to each pixel cell (Fig. 11) to compensate for the parasitic diode leakage of the switch. The compensation PN diode is made from half of a PMOS transistor (body diode) to yield a close match with the switch leakage current when V_{Dbias} is applied externally. In equation (8), V_{Droop} must be less than 1 LSB in order to preserve information for 10msec of hold time maximum. n is the number bits of accuracy. Substituting (10) into (9), the droop can be determined. From (9) and (10), the droop is minimized and accuracy maintained if both I_{Dleak} and I_{swleak} are closely matched.

$$V_{Droop} < \frac{V_{store}}{2^{n+1}} \tag{8}$$

$$V_{Droop} = \frac{\Delta I_D}{C_{store}} t \tag{9}$$

$$\Delta I_D = I_{Dleak} - I_{swleak} \tag{10}$$

Since the diode leakage doubles every $5^{o}C$, equation (10) can be re-written as in (10.1). Assuming an operational temperature of $100^{o}C$, room temperature at $25^{o}C$ and a local mismatch of 2%. With V_{store}=1.5V, C_{store}=1.1pFd, t=10msec, $\Delta T = 75^{o}C$ (the difference between room temperature and operation temperature) and n=10 (the number bits of accuracy), the I_s at room temperature can be calculate as follows:

$$\Delta I_D(T) = I_{Dleak} 2^{\frac{\Delta T}{5}} - I_{swleak} 2^{\frac{\Delta T}{5}} = 2^{\frac{\Delta T}{5}} \Delta I_{room} \tag{10.1}$$

$$\Delta I_D(100) = 2^{75/5} \Delta I_{room} = 32768 \times \Delta I_{room} \tag{11}$$

$$I_\varepsilon = \Delta I_D < \frac{V_{store} C_{store}}{t 2^{n+1}} \tag{12}$$

$$I_s = \frac{\Delta I_D 50}{2^{\Delta T/5}} \tag{13}$$

With the predicted diode saturation current of 1.23×10^{-16} from equation (13), the measured value from testing can be verified with the predicted value to determine of the droop rate effects accuracy.

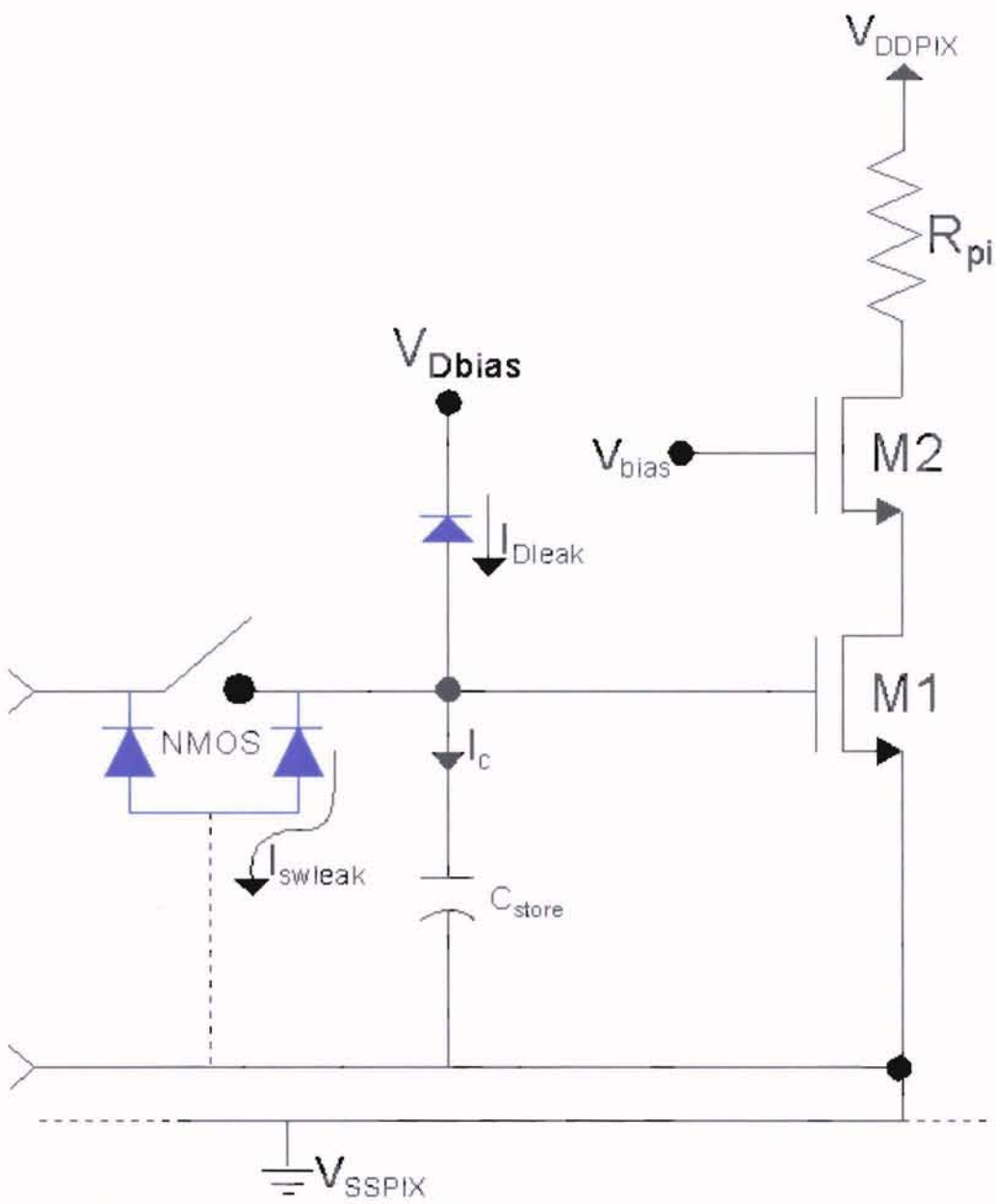

Fig. 11: Schematics of the additional compensation diode to balance the leakage current of the column switch to the substrate

3.3 NONLINEARITY ISSUE

The operational temperature dependencies of the pixel resistor, and process parameters are the factors that affect the write performance and accuracy. The pixel resistance changes with temperature, which is modeled by the thermal coefficient of resistance (TCR) of poly of 0.05% per ^{o}C [13]. With this and application temperatures approaching 250 ^{o}C in mind, the pixel resistance can easily increase by more than 10%. Emission is a function of current, resistor value, effective temperature, and layout geometry. The amount of the IR emission is proportional to the temperature, which is proportioned to square of input current and the pixel resistance. The black body effect of R_{pix} is a function of temperature, which is proportional to the fourth power of its absolute temperature [14]. Also the pixel heating causes localized temperature changes in substrate in turn reducing the threshold voltage and mobility of transistors thus lower the amount of current (M1) supplied to the pixel emitter. As a result of these combined effects each pixel will not remain linear with pixel current over the full 9-10 bits of dynamic range.

Pixel thermal cross talk is another factor that increases the complexity of IR emission nonlinearity. Thermal Cross talk occurs between pixels as a result of incomplete thermal isolation. Each pixel is effected by the neighboring pixels depending on the image pattern and scene by scene basis. The temperature associated with the IR emission causes a number of variations thus increase the complexity of the nonlinearity. The increase or decrease in temperature results in the following parameter variation:

- The pixel resistance may increase by more than 10%
- The current may reduce as much as 25% caused by the decrease in mobility
- Thermal (IR) emission is proportional to T^4 of the pixel
- The thermal cross talk between local pixels effects the pixel electronics

One fortunate turn of events is that thermal emission increases with the increase in R_{pix} but cascode current decreases with the increase in MOS temperature.

For future applications a model taking into consideration thermal cross talk and pixel emission model, which incorporates I, R, T_e, and geometry or topology must also be included to characterize the pixel performance. An emission look up table can be generated from the measurements on an n by n array of pixels. The look up table and the model should then be verified through experimentation. Once the table is generated from the model, IR emission scene accuracy can be improved through the use of tables to find the desired current level, which correspond to the desired emission levels. Future application will utilize this offline image pre-warp or compensation on a scene by scene eliminating nonlinearity.

The write, droop and nonlinearity issues were discussed in this chapter to ensure the accuracy and the performance of the RITR chip. The write accuracy was improved by adding the return reference path to eliminate IR drop. The droop was minimized by the addition of a compensation diode. Cascoded transistors were used to increase the output impedance thus assuming a more constant current sink operation. With regard to thermal issues, which are not well modeled an in-depth investigation, analysis and measurements should be done in any continuance of this project.

CHAPTER 4

RTIR CHIP TEST RESULTS

The test set employing RTIR technology will yield a high payoff by improving the assessment of IR systems availability and operability. This RTIR capability will reduce the number of test systems in the maintenance chain for IR sensors, therefore lowering the overall system operation cost. The use of RTIR as built-in-test-equipment (BITE) will further improve readiness testing of expensive sensors and weapon systems. Each key circuits were laid out as test cells to debug and verify the functionality of the circuits incase the chip fails to operate. The diode leakage from the minimum geometry switch was measured. The expected leakage current was calculated from the data to predict high temperature droop. The cascoded transistor was measured to determine its bias voltage and verify the ideality of current sink operation. The thermal pixel array (TPA) system was packaged by TITAN Corp. and tested by both the TITAN and SPAWAR, and the cells by OSU. The radiometric measurements were the contribution of Bruce Offord, Ronald Marlin, and Richard Bates from the SPAWAR teams. The scene generation was the contribution of Gordon Perkins from TITAN Corporation.

4.1 BULK DIODE MEASUREMENT

An NMOS minimum geometry body diode was probed and its saturation current (I_S) was measured at room temperature, see in Fig. 12. The saturation current is temperature dependent with current roughly doubling every $5\,^{o}C$. From this property, the current at high temperature can be estimated. At $25\,^{o}C$, $V_T = \frac{kT}{e} = 25.7mV$ with the ideality factor n=1 and I_d=2.54x10^{-13}A, the saturation current (I_S) can be determined from equation (14). A slope fit was used to determine the y-axis intercept for the $Ln(I_D) = -30$ and to estimate a saturation current at room temperature equal $9.36x10^{-14}$ A. This in turn yields a droop rate projection. From the previous chapter, an estimate for the desired saturation current yielded 1.23x10^{-16}A. The measured saturation current is then plug back into (12) and (13) in chapter 3 to find the real number bits of accuracy achieved and yielded n<1 with the temperature at $75\,^{o}C$. To ensure 9 or greater bits of accuracy from (12) and (13), the substrate temperature must be limited to below $52\,^{o}C$.

$$I_D \approx I_S \exp\left(\frac{V_D}{nV_T}\right) \tag{14}$$

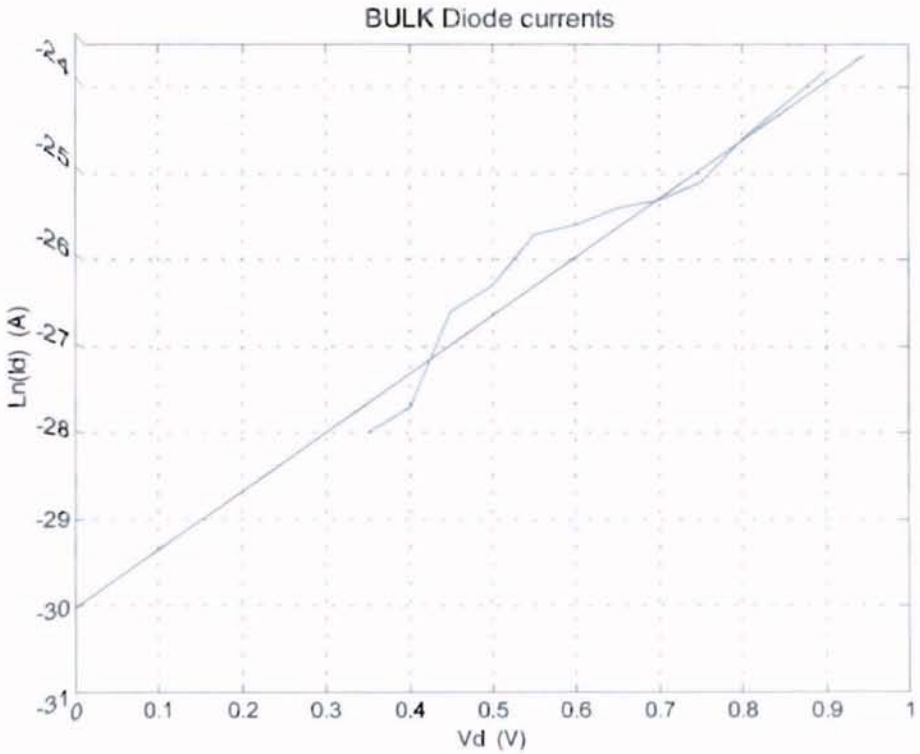

Fig. 12: BULK body diode current-voltage curve

4.2 CASCODE MEASUREMENT

The cascoded transistor was tested to determine the bias voltage (V_{bias}) with the test structure shown in Fig. 13. It was experimentally determined that a bias voltage of 2.1V would best ensure the proper operation of the cascoded transistor during pixel operation. The bias voltage was then held constant with the stepping up of input voltage and sweeping of the drain to source voltage. Fig. 14 shows the I_D - V_{DS} characteristic of the cascoded device as it operates in the pixel design. Note that the drain current remains nearly constant from 1.5V to 5V with a measured output impedance of 1.2MegΩ at the worst case current of 500μA. Test data verifies that the cascoded device provided the desired output impedance as required by the design specification. The one MegΩ plus in conjunction with a pixel voltage of 8 volts results in less than an 8 μA error. This is 12dB of magnitude below the 16μA required to develop a quantum of pixel power which is more than adequate to meet the requirements for 10 bits of dynamic range.

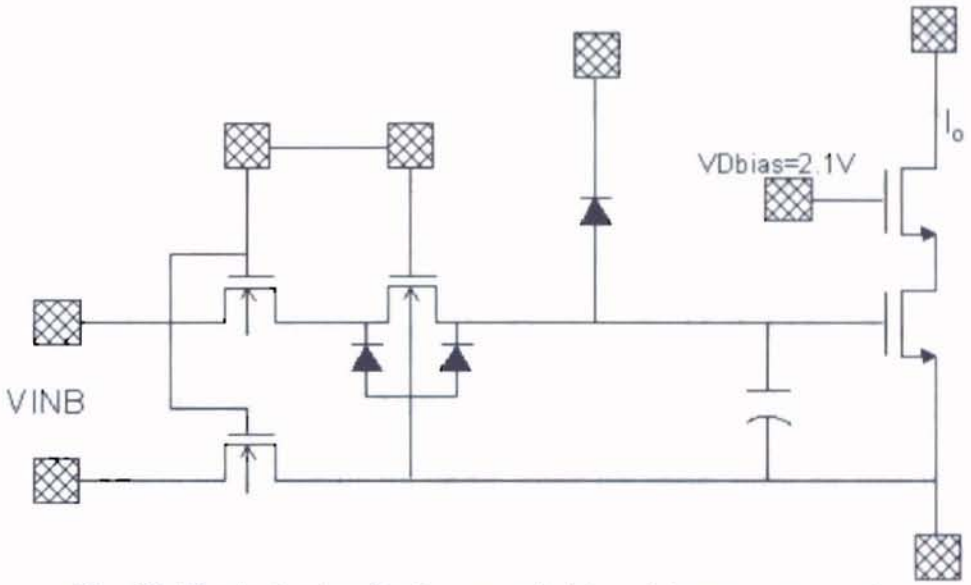

Fig. 13: The test setup for the cascoded transistor measurement

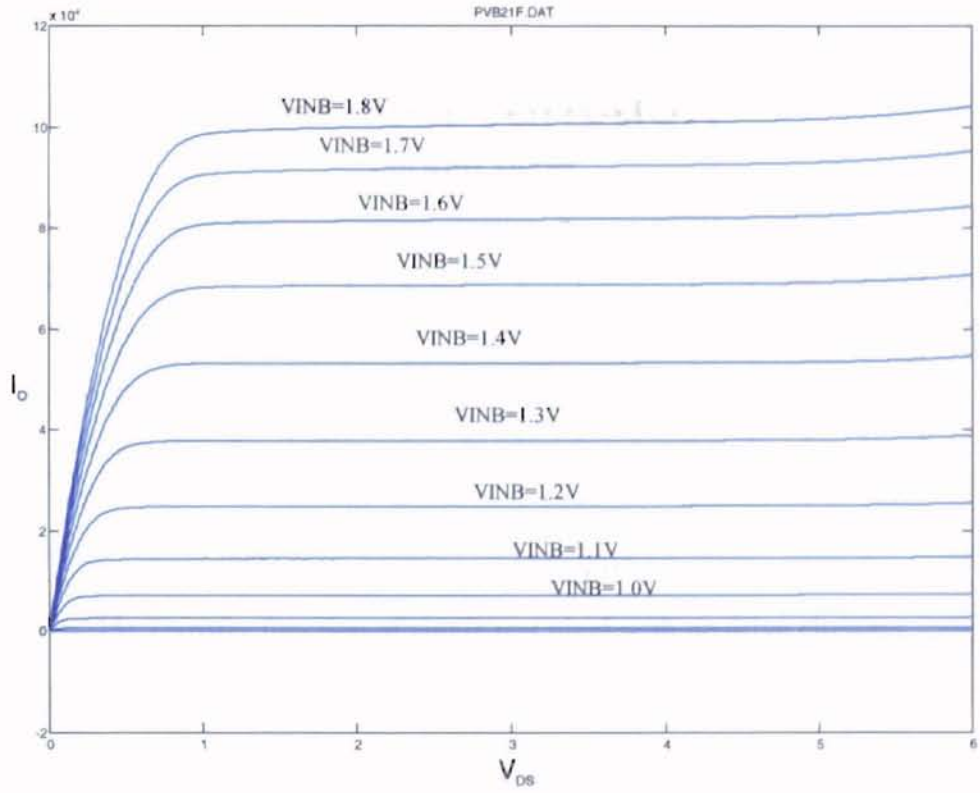

Fig. 14: V_{DS} vs I curve of the cascoded transistor at V_{bias}=2.1V

4.3 Radiometric measurements

Measurements of the infrared radiant characteristics for 20 by 20 μm heaters were made using a 4- to 5.5- μm filter [15, 16]. Fig. 15 shows the transfer function for a single pixel without its driver circuit. The effective pixel temperature is plotted against the applied power. The data were taken with a microradiometer, which had an effective aperture of 67 microns, and was calibrated using a cavity black body. The data were corrected for the smaller area of the heaters and for an effective fill factor [16], which is approximately 50% of the geometric fill factor. Since the heater filled the field of view of the microradiometer, the temperatures are averaged over the heater surface. The peak temperatures of the pixel trampoline were estimated to be 50 C^o higher.

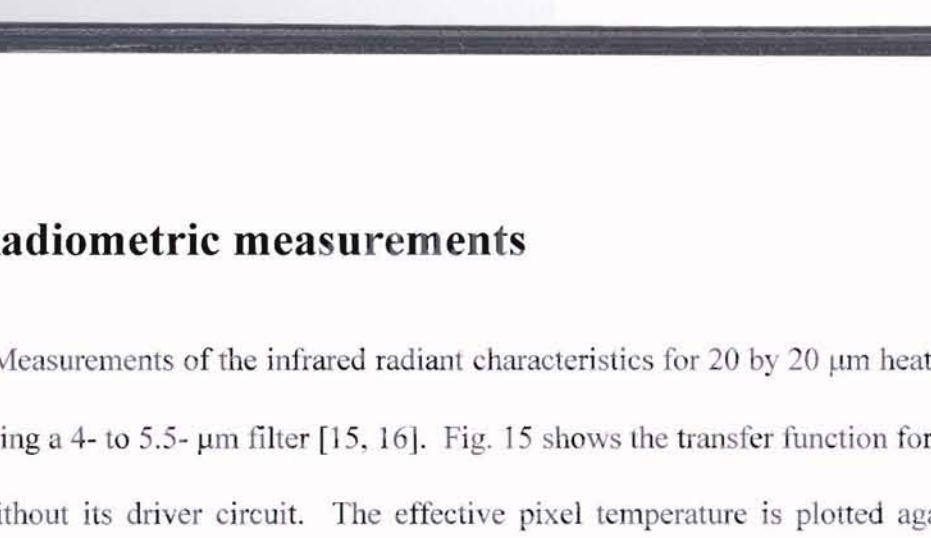

Fig. 15: Transfer function of single test pixel with no drive circuitry

Fig. 16 shows oscilloscope traces of rise and fall characteristics of the same 20 by 20 μm pixel. The heater was driven by a square wave from a constant current source, and

the microradiometer with 4- to 5- μm band pass filter was used to measure the radiant output. The result shows the rise time (10% - 90%) is less than 2msec with a fall time less than 1msec with the average thermal time constant being 1.5msec by taking the average of the rise and fall time.

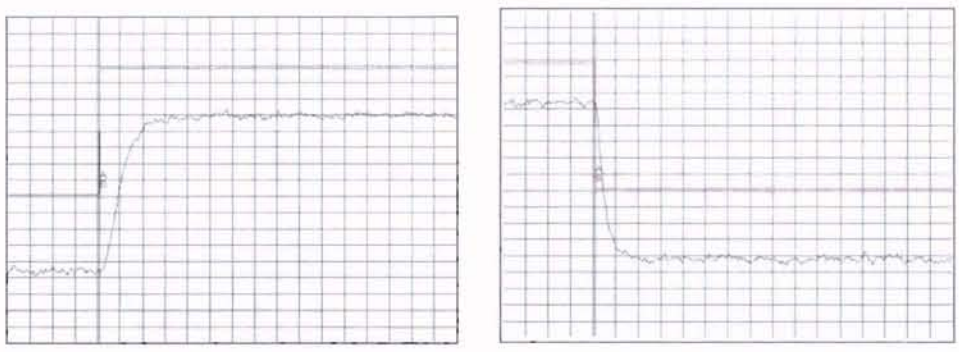

Fig. 16: Rise and fall times for single test pixel (8k Ω) with no drive circuitry

A measurement of the hold time for the 128 by 128 pixel array with sample-and-hold circuitry, and V_{bias}=1.5V and V_{Dbias}=3.5V is shown in Figure 17. The array was driven at a refresh rate of one frame per 20 seconds, and tested with a lock-in amplifier having a time constant of 30 msec to measure the hold time. A refresh rate of one frame per five seconds was also used to expand the time scale to better show the decay. The decay time to 90% of peak was in the range of 0.25 to 0.5 seconds. The decay function is shown in (15). Using (15) the time constant was determined to range from 2.4 to 4.8sec.

$$0.9V_{peak} = V_{peak}e^{-1/\tau} \tag{15}$$

$$0.9V_{peak} = V_{peak}e^{-t/\tau} \tag{15}$$

$$1 - e^{-t/\tau} = \frac{1}{2^n} \tag{16}$$

Using (16) and solving n,

$$n = -\frac{\ln(1 - e^{-t/\tau})}{\ln 2} \tag{17}$$

the number bits of accuracy is 7.9 and 8.9 bits for 250msec and 500msec respectively.

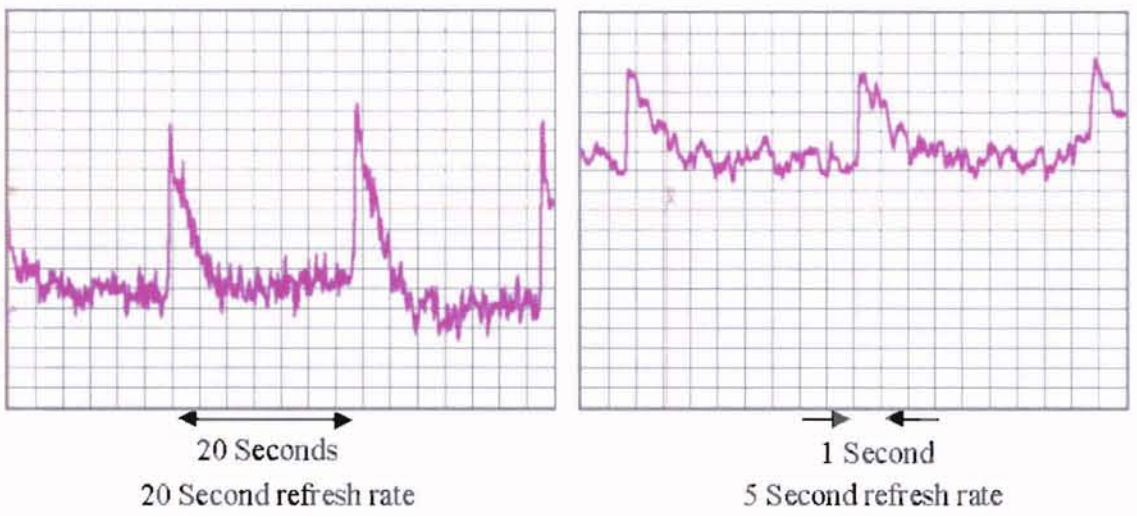

Fig. 17: Hold times for heater in a 128 X 128 array

For this setup, the diode bias (V_{Dbias}) was set at 3.5V. With additional experiments, the droop performance was improved by setting V_{Dbias} around 5V, which suggests improved an accuracy of 9-10 bits. Experimental observations have shown that the full array operates best with V_{Dbias} near 5V. This may be due to the voltage drop associated with 16,000 pixel currents, or the compensation diode mismatching.

4.4 SCENE GENERATION

To demonstrate and characterize a completed TPA, a support system was developed by TITAN (Fig. 18) that pre-processed and stored IR images on high speed storage drives to support real time IR scene generation. In keeping within the low cost spirit of the program, Commercial Off-The-Shelf (COTS) solutions have been incorporated whenever possible. The TPA support system consists of two major components. First, a system to format and deliver dynamic digital infrared movies and second, a system to house and provide all the necessary electronics to bias and drive the TPA device.

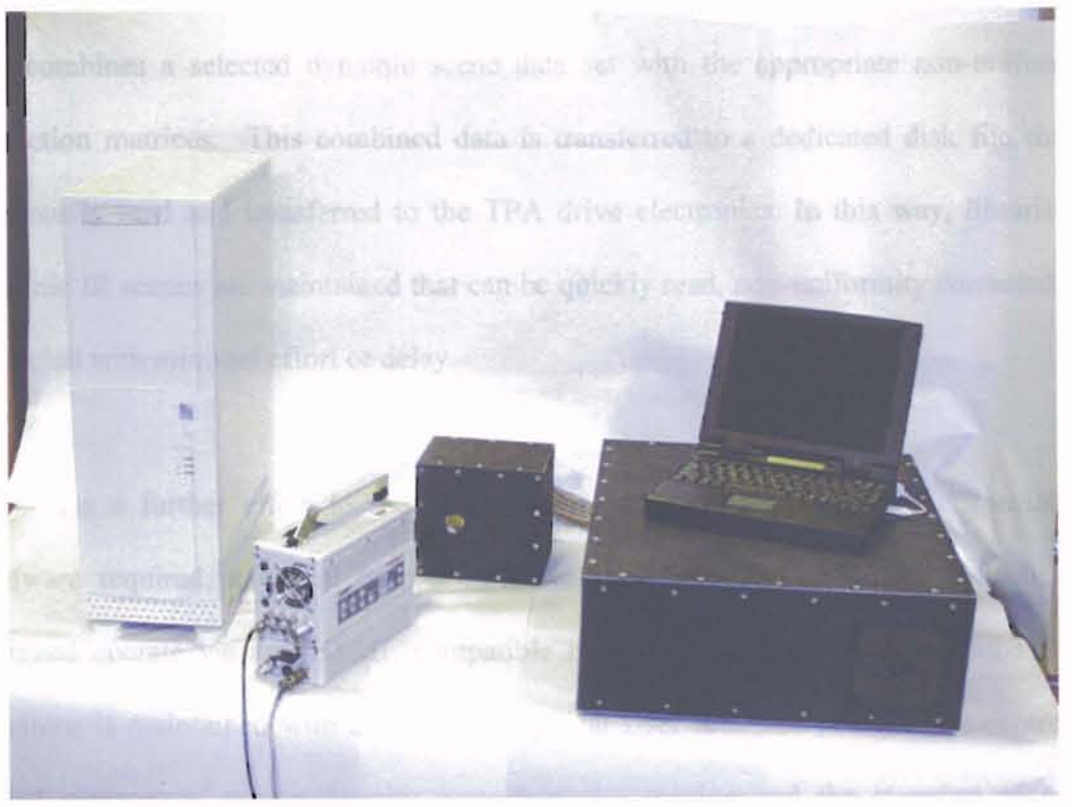

Fig. 18: The TPA system setup (courtesy of TITAN Corp.)

The support system electronics is able to control global aspects of the system such as; the TPA set point temperature, image brightness and image contrast. Additionally, the system is required to monitor the actual operating temperature of the TPA. The support system electronics is capable of providing 128 by 128 by 16 bit pixel images at frame rates of one hundred images per second.

The approach to support system design was to integrate standard and general-purpose PC hardware wherever possible and limit new hardware design and construction only where needed to bias and drive the TPA. All infrared movie files were computed in advance and archived to high-performance disk. Additional data files are maintained for non-uniformity correction. To project a synthetic infrared scene, a process is invoked that combines a selected dynamic scene data set with the appropriate non-uniformity correction matrices. This combined data is transferred to a dedicated disk file that is continually read and transferred to the TPA drive electronics. In this way, libraries of dynamic IR scenes are maintained that can be quickly read, non-uniformity corrected and projected with minimal effort or delay.

As a further effort to reduce development cost and minimize the specialized hardware required, a virtual user console was developed. This virtual console was designed operate via any HTML compatible browser. Complete control of the RTIR functions is maintained with a familiar Graphical User Interface (GUI). The control of global parameters, non-uniformity correction, the starting and the stopping of scene projection, and all online documentation and support are all readily accessible via the

HTML interface (Fig. 19). The IR images displayed on the RTIR IC are shown in Fig. 20 and 21.

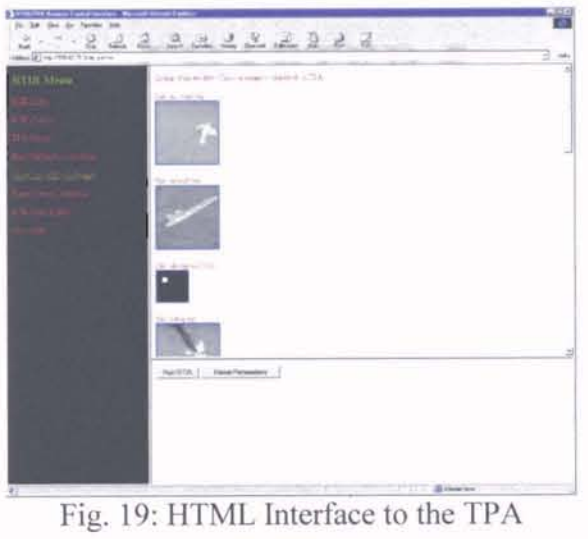

Fig. 19: HTML Interface to the TPA

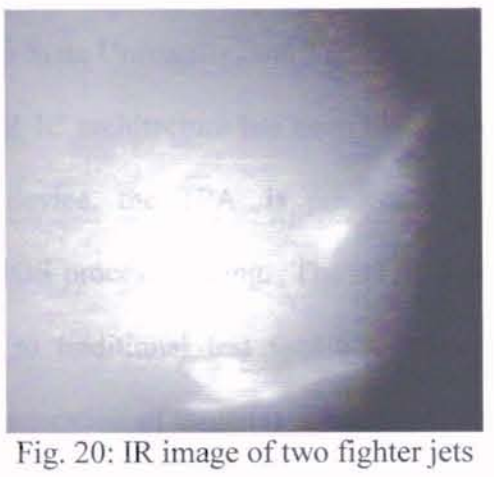

Fig. 20: IR image of two fighter jets

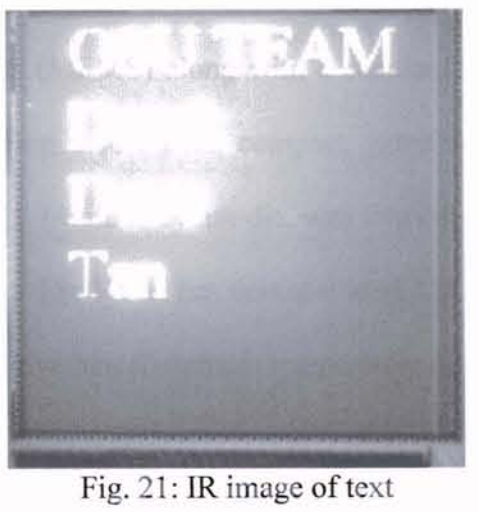

Fig. 21: IR image of text

CHAPTER 5

CONCLUSIONS

The real-time infrared (RTIR) IC is a joint project developed by SPAWAR System Center, Oklahoma State University, and TITAN Systems Corporation. The 128 x 128 scene generator RTIR IC architecture has been described with each key component discussed. A MEMS device, the TPA, is produced using state-of-the-art CMOS technology with post CMOS process etching. The RTIR system provides a low-cost yet high fidelity alternative to traditional test facilities. The RTIR IC offers real-time dynamic thermal scene generation of target(s) against/in background scenes for viewing by current and future IR sensors. The project goal was to utilize Micro Electromechanical Systems (MEMS) along with a standard commercial silicon CMOS-based technology to develop a low cost, compact, portable and yet rugged IR scene generator. The IR array IC, 14mm x 14mm die, was fabricated in the Supertex (formerly Orbit) 1.2 micron process. The RTIR has demonstrated 128 x 128 array operation at up to 100Hz and with an effective heater element temperature of 500Kelvin.

Micro-heaters were scaled to 40μm x 40μm to meet the requirements for an IR scene generator integrated circuit, and compatible with standard CMOS processing. Drive electronics have been developed to provide arbitrary real time infrared video scenes. Although this monolithic approach cannot attain the density of pixels that can be had using a bump bonded or other hybrid approaches, it has the advantage of simplicity, low cost, and non-proprietary technology.

As the test data showed in chapter 4, the cascoded transistor has an output impedance of 1.2MegΩ at a worst case to full scale resulting in less than ¼ of a bit of degradation in accuracy. The compensation diode provides a saturation current of 9.36×10^{-14}A at room temperature. A droop accuracy of greater than 9 bits can be achievable by holding the substrate temperature below $52^{o}C$ embed Equation 3. The decay time to 90% of peak was in the range of 0.25 to 0.5 seconds from hold time measurements resulting in a time constant in the range of 2.4 to 4.8 seconds. As a result 7.9 to 8.9 bits of accuracy were achieved. In summary, with the bit degradation error from both the cascoded transistor and diode leakage current taken into consideration and with an operation temperature less than $50^{o}C$ embed Equation 3, better than 8 bit of accuracy was achieved.

As future improvements, the length of the cascoding drive transistor should be increased as the pixel area allows addressing the issue of the low output impedance. A more detailed analysis along with experimentation must be done to improve or find the limits of localized matching of the MOS diodes. A model must be developed to address the issues characterize the nonlinearity IR emission behavior of the pixel. As a result of

model availability, offline image pre-warp or compensation on a scene by scene can be applied to minimize or eliminate pixel IR nonlinearity.

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